PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Jiunn-Ren Hwang, Anseime Chen, I-Hsiung Huang
Examiner: Ruggles, John S
Filing Date: 05/10/2001
Art Unit: 1756
Serial No.: 09/851,580
Docket No.: NAUP0292USA

Title: METHOD OF FORMING STORAGE NODES IN A DRAM

To: Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Subject: Information disclosure statement Under 37C.F.R.§1.56 and 37C.F.R.§1.97(b).

Dear Sir:

This is an Information Disclosure Statement in accordance with the duty to disclose information material to patentability under 37 C.F.R. §1.56. Applicants wish to make of record the document listed on the accompanying form PTO/SB/08. It is respectfully requested that the Examiner initials the cited reference on the form and that it be made of record in the application and that a copy of the initialed form be sent to Applicants with the next communication from the Examiner.

Since the information disclosure statement is filed

after the filing of a request for continued examination under §1.114, the requirement set forth in §1.97(b)(4) is satisfied. The prior art patent contained in the information disclosure statement was cited in communications from the China Intellectual Property Office on 09/25/2003. Applicant sincerely hopes that the examiner can consider the item contained in the information disclosure statement.

According to the requirement set forth in 37C.F.R.§1.98 and M.P.E.P. 609 (8th edition, Aug. 2001), the applicant is submitting copies of the reference cited by the China Intellectual Property Office (Japan Publication No. JP 9-8240A, published Jan. 10, 1997) and a concise explanation of the relevance in this application hereinafter.

Japan Publication No. JP 9-8240A discloses a method of forming electrodes 12a. The method includes to form an electrode layer 12 on a substrate 11 first. Then, a photoresist layer 13 is formed on the electrode layer 12. Expose the photoresist layer 13 with a first mask 21 to form a first line pattern 23a (refer to Fig.(1) of the cited prior art). After that, expose the photoresist layer 13 with a second mask 31 to form a second pattern 33a crossover with the first line pattern 23a (refer to Fig.(2) of the cited prior art). A development process is thereafter performed to form "island patterns" 13a in the photoresist layer 13 (refer to Fig.(3) of the cited prior art). Finally, the electrode layer 12 is etched by utilizing the island patterns 13a as a mask to form electrodes 12a

(refer to Fig.(4) of the cited prior art).

Claim 1 of the present application is repeated here for reference:

"1. A method of forming storage nodes in a dynamic random access memory (DRAM) on a semiconductor wafer, the semiconductor wafer comprising a substrate, a thin film layer positioned on the substrate, and a photoresist layer positioned on the thin film layer, the method comprising:

performing a first exposure process to form first exposure regions **that are lines parallel with each other on the photoresist layer;**

performing a second exposure process to form second exposure regions **that are rectangles interlaced with and perpendicular to each other on the photoresist layer, and the second exposure regions doing not overlap the first exposure regions;**

performing a development process on the first exposure regions and the second exposure regions of the photoresist layer;

removing the first exposure regions and the second exposure regions of the photoresist layer to form an array photoresist layer on the thin film layer; and

using the array photoresist layer as a mask to perform an etching process to remove portions of the thin film layer not covered by the array photoresist layer so as to form an array thin film layer, the array thin film layer being used as the storage nodes in the DRAM."

Compared with Japan Publication No. JP 9-8240A, the present application method of forming storage nodes in a DRAM is to provide a semiconductor wafer 60 first. The semiconductor wafer 60 comprises a silicon substrate 62, a dielectric layer 63 on a surface of the silicon substrate 62, a plurality of node contacts 64 in the dielectric layer 63, an amorphous silicon layer 65 positioned on a surface of the dielectric layer 63 and covering each node contact 64, and a photoresist layer 67 positioned on a surface the semiconductor wafer 60 (refer to Fig.10 of the present application).

Then, a double exposure process is performed to form photoresist patterns 69 by utilizing a mask 71 and a mask 75. The first exposure process is performed to transfer a mask pattern 73 onto the photoresist layer 67 by utilizing the mask 71. **The mask pattern 73 comprises a plurality of non-intersecting opaque bands, and each of the bands covers an area that corresponds to positions of a plurality of photoresist patterns 69 on the semiconductor wafer 60.** A second exposure process is thereafter performed to transfer a mask pattern 77 onto the photoresist layer 67 by utilizing the mask 75. **The mask pattern 77 of the mask 75 comprises a plurality of rectangles interlaced with and perpendicular to each other, and each rectangle corners positioned on the storage nodes. That means, the opaque areas of the mask pattern 77 cover the areas that correspond to the positions of the photoresist patterns 69 (refer to Fig.11 to 13 of the present application). The s miconductor wafer 60 is then**

plac d into a d v loper to und rgo a development proc ss.

After the development process is completed, several rinse processes are then performed to remove dissolved photoresist and the developer. After the exposure, development, and rinse processes, the plurality of photoresist patterns 69 are formed on the semiconductor wafer 60. An etching process is then performed to remove portions of the amorphous silicon layer 65 not covered by the photoresist patterns 69 down to the surface of the dielectric layer 63 to form storage nodes 70 by utilizing the photoresist patterns 69 as a hard mask during the etching process (refer to Fig.14 of the present application).

In summary, the present application uses the mask 71 to form a plurality of lines parallel to each other and covering each storage node followed by an exposure process using the mask 75 to cut the lines covering storage nodes to form a plurality of the array photoresist patterns 69. Therefore, optical proximity effects cause underexposure on areas of the photoresist layer 67 that correspond to the corners of a transparent area 80 when a light beam penetrates through the transparent areas 80 on the mask 75 to the photoresist layer 67 during the exposure process. **The formed photoresist patterns 69 possess slightly enlarged corners due to underexposure**, and so the size of the formed photoresist patterns 69 is also slightly larger than that of the design patterns. These slightly larger photoresist patterns 69 not only compensate for

losses in the amorphous layer during the etching process, but also compensate for the reduction in size of the storage node in the subsequent resin process.

It is clear that portions of the photoresist layer 13 are exposed twice, leading to a plurality of overexposure areas between island patterns 13a in the patent cited by the China Intellectual Property Office. This overexposure tends to have more severe optical proximity effects, which in turn round corners of the adjacent island patterns 13a. Since the size of the island patterns 13a is smaller than that of the design, the size of the subsequently formed electrodes 12a are therefore smaller than the design size.

Since claim 1 of the present application is substantially different from the prior art patent Japan Publication No. JP 9-8240A, and all other claims are dependent on claim 1, a quick allowance of the present application is sincerely requested.

Respectfully Submitted,

Winston Hsu Date: 12/15/2003

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PTO/SB/08A (10-01)
Approved for use through 10/31/2002. OMB 0651-0031
U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet 1 of 1

Complete if Known	
Application Number	09/851,580
Filing Date	05/10/2001
First Named Inventor	Jiunn-Ren Hwang
Art Unit	1756
Examiner Name	Ruggles, John S
Attorney Docket Number	NAUP0292USA

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number - Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
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FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3] -Number[4] - Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]
	1	JP 9-8240 A	01-10-1997			+

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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